Tutorial for students:

For using modelsim, first, you have to have your VHDL files in some directory.

1. Click the icon of modelsim in Windows environment (or type VISM in Unix environment). It will give you a window as following:

ModelSim XE II/Sta	arter 5.7c - (Custom Xilinx Versio	n	
File Edit View Compile	e Simulate To	ools Window Help		
] 😅 🛍 🛍 🖬 🛛 🕸	🏥 🏹 🐹			
Workspace				
Name	Туре	Path		<u> </u>
	Library able) Library Library lable) Library Library Library	\$MODEL_TECH//xilin> \$MODEL_TECH//xilin> \$MODEL_TECH//xilin> \$MODEL_TECH//xilin> \$MODEL_TECH//xilin> \$MODEL_TECH//xilin>	<td></td>	
# Reading C:/Modeltech_ # Loading project adder ModelSim>	_xe_starter/tcl/v:	sim/pref.tcl		
Project : adder <no< td=""><td>Design Loade</td><td>d></td><td><pre><no context=""></no></pre></td><td></td></no<>	Design Loade	d>	<pre><no context=""></no></pre>	

2. Click File \rightarrow New \rightarrow Project \rightarrow type in Project Name(counter) \rightarrow Click Browse to select the location that you want(C:\minhua\spring2007\csc343\M4counter).

🕅 Create Project 🛛 🔀			
Project Name			
Project Location			
/spring2007/csc434/M4counter Browse			
Default Library Name			
work			
OK Cancel			

3. Click OK to get the window as following:

A	dd items to the Project	×		
	Click on the icon to add items of that type:			
	Create New File Add Existing File			
1	Close	,		

4. Select Add Existing File. (I select the existed VHDL files: M4counter.vhd and test_M4counter.vhd)



5. Compile these two files: high-lighten the M4counter.vhd \rightarrow compile \rightarrow compile all



6. If your code has no syntax error, it will show a window as following:



7. In the window above, double click Library → click '+' next to work → double click test_M4counter → it will get a window as following:

Workspace			×
▼ Name	Туре	Path	*
□ work	Library	C:/minhua/spring2007/csc434/M	
C] cfg_tb	Config	C:/minhua/spring2007/csc434/M	
∯-Ē] m4counter	Entity	C:/minhua/spring2007/csc434/M·	
	Entity	C:/minhua/spring2007/csc434/M·	
⊡– ∭ , aim	Library	\$MODEL_TECH//xilinx/vhdl/aim	
📠 aim_ver (unavailable)	Library	\$MODEL_TECH//xilinx/verilog/a	
œ cpld	Library	\$MODEL_TECH//xilinx/vhdl/cpl	
🔲 🃠 cpld_ver (unavailable)	Library	\$MODEL_TECH//xilinx/verilog/c	
œ ⊥ ns	Library	\$MODEL_TECH77xilinx7vhdl/pls	
⊡ simprim	Library	\$MODEL_TECH77xilinx7vhdl/sim	
📠 simprims_ver (unav	Library	\$MODEL_TECH//xilinx/verilog/s	
👖 uni9000_ver (unava	Library	\$MODEL_TECH//xilinx/verilog/u	
⊞– ∫ unisim	Library	\$MODEL_TECH77xilinx7vhdl/uni	
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	Library	\$MODEL_TECH77vital2000	
	Library	\$MODEL_TECH77xilinx7vhdl7xilir	
xilinxcorelib_ver (un	Library	\$MODEL_TECH//xilinx/verilog/>	
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⊕_,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Library	\$MODEL_TECH//modelsim_lib	
	Lihraru	\$MODEL_TECH/_/std	-
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8. click View → Signal → Wave , Click Edit (in the signals window) → Select All → drag all signals into wave window.

	🔢 wave - default		王國医
 Vame t_reset t_inc t_clock t_count 	 /test_m4counter/t_re No Data /test_m4counter/t_inc No Data /test_m4counter/t_cl No Data 		
	Now	800 ns	600
	Cursor 1	0 ns <mark>0 ns</mark>	

📻 wave - default					+ 2	×
/test_m4counter/t_re	0	٦				$\overline{\lambda}$
/test_m4counter/t_inc	0					
/test_m4counter/t_cl	0		nnn			
	00	<u>00)(01)(10)(11</u>	<u>/00/01/00/11</u>	(10)(01)(00		
						7
Now	800 ns					ŕ
Cursor 1	Ons	0 ns	00 41	0 0	00	
						-
U ns to 726 ns		Now: 800 n	is Delta: U			
] 📰 wave 📊 test_M4count	er.vhd					€ >
						- 7

9. In the main window, click Simulation \rightarrow Run 800ns \rightarrow Run All \rightarrow click