```
library ieee;
use ieee.std_logic_1164.all;

entity test_Dlatch is
end test_Dlatch;


architecture TB of test_Dlatch is

    component D_latch
    port(   D:                in std_logic;
            enable:           in std_logic;
            Q:                out std_logic
    );
    end component;

    signal T_D:   std_logic;
    signal T_enable:    std_logic;
    signal T_Q:           std_logic;

begin

    U_latch: D_latch port map (T_D, T_enable, T_Q);

    process

      variable err_cnt: integer := 0;

    begin

      T_D <= '1';
      T_enable <= '0';
      wait for 10 ns;

      -- case 1
      T_enable <= '1';
      wait for 2 ns;
      assert(T_Q='1') report "Error1!" severity error;
      if (T_Q/='1') then
          err_cnt := err_cnt + 1;
      end if;

      -- case 2
      T_D <= '0';
      wait for 15 ns;
      assert(T_Q='0') report "Error2!" severity error;
      if (T_Q/='0') then
          err_cnt := err_cnt + 1;
      end if;

      -- case 3
      T_D <= '1';
      wait for 15 ns;
      assert(T_Q='1') report "Error3!" severity error;
      if (T_Q/='1') then
          err_cnt := err_cnt + 1;
      end if;
```

```
      -- case 4
      T_enable <= '0';
      T_D <= '0';
      wait for 2 ns;
      assert(T_Q='1') report "Error4!" severity error;
      if (T_Q/='1') then
          err_cnt := err_cnt + 1;
      end if;

         -- case 5
        T_D <= '1';
      wait for 15 ns;
      assert(T_Q='1') report "Error5!" severity error;
      if (T_Q/='1') then
          err_cnt := err_cnt + 1;
      end if;


      -- case 6
      T_enable <= '1';
        T_D <= '0';
      wait for 2 ns;
      assert(T_Q='0') report "Error6!" severity error;
      if (T_Q/='0') then
          err_cnt := err_cnt + 1;
      end if;

      -- summary of all the tests
      if (err_cnt=0) then
          assert false
          report "Testbench of Adder completed successfully!"
          severity note;
      else
          assert true
          report "Something wrong, try again"
          severity error;
      end if;

      wait;

    end process;

end TB;

configuration CFG_TB of test_Dlatch is
      for TB
      end for;
end CFG_TB;
```