# Register File Lab

What to do:

1) Read item 7. Register File on the lab page of the class website to understand how the register file works.

   Notice that *registerfile.vhd*, provided in the above document, uses components *dff*, *decoder*, *AND1*, and *multiplexor4*.

2) Create the appropriate vhd files for each of the above components.

3) Create a test file for the *registerfile.vhd*.

4) Simulate your code in ModelSim to verify that the logic is correct.

5) Create a new project in Quartus with a block diagram that uses symbols for *DEBOUNCE*, *CLK_DIV* (both are provided in the *Rapid Prototyping* cd), *Scounter* (use an LPM_counter or *count4* provided by MinHua), *Multiplexer* (using LPM_mux or your own design for a 4 input mux), *registerfile*, and *LCD_Display* (provided by the lab book cd, but must be modified to output your results). Refer to the diagram in the Register File pdf.

6) Simulate your design in Quartus to verify accuracy.

7) Download your design onto the UP3 Board.

8) Create a *new* project in Quartus replacing the *registerfile* symbol with an LPM_RAM_DP. This is a dual-port ram, which works very similarly to the register file. However, this LPM module allows you to read from *only one address*. It also allows you to write data to an address. (You will not be using this capability.) Look at the Quartus Help file for more information about the LPM_RAM_DP module.

9) Simulate your design to verify accuracy.

10) Download your design onto the UP3 Board and verify that the LMP module works the same as *registerfile*.