Quartus Tutorial: 8-bit 2-1 Multiplexer on the MAX7000S Device

Before you begin:

Create a directory in your home workspace called *csc343*. **Note**: You will use this folder to store all your projects throughout the semester.

Copy the files *DEC_7SEG* and *mux_2input_pin_assignment* from the course website into the directory you just created.

- 1. Open Quartus II: Open a Linux/Unix terminal and type quartus.
- 2. Create a new Quartus project (.qpf):
 - 2.1. Click File -> New Project Wizard.
 - 2.2. Click *Next* at the bottom of the **New Project Wizard: Introduction** page. *You will now be on page 1 as shown below.*

	picitus.		
What is the name of this pro	ject?		
mux_2input			
What is the name of the top and must exactly match the	level design entity for th entity name in the design	is project? This nar n file.	ne is case sensitive
mux_2input			
Use Existing Project Settin	gs		

- 2.3. Specify the working directory:
 - a) Click the ... button to the right of field (a) in the figure above to browse for the *csc343* directory you created above.

The path to this directory will be shown in field (a).

- b) Type *mux_quartus* after the path that was just displayed in field (a). Note: This directory does not exist, but Quartus will make it for you.
- c) Specify the project name: Type *mux_2input* in field (b). Quartus automatically names the top-level design in field (c) the same as the project name.
- 2.4. Click *Next* at the bottom of page 1 of the **New Project Wizard**. *You will be on page 2 as shown below*.

File name		Туре	Add All
			Remove
			Properties
			Up
			Down
Specify the path name	s of any non-default librari	es. User Libra	ries
specity the patriname	s of any norradiatik librar		iies

- 2.5. Click the ... button to the right of field (a) in the figure above to browse for the file *DEC_7SEG*, then click *OK*.
- 2.6. Click *Add*, then click *Next* at the bottom of page 2 of the **New Project Wizard**. *The You will now be on the* **Family & Device Settings** *page as shown below*.

ew Project Wizard: Family & Device Settings [page 3 of 5]						
Select the family and device you want to target for compilation.						
Family: MAX7000S						
Target device C Auto device selected by the Fitter from the 'Available devices' list Specific device selected in 'Available devices' list						
Available devices:		- Filters				
EPM7128SLC84-7 EPM7160SLC84-7		Package:	Any			
		Pin count:	84			
		Core voltage:	5.0V			
		🔽 Show Adv	anced Devic	es		
		Companion de	evice			
		HardCopy II:	DAM - U			
Limit DSP & HAM to HardLopy II device resources						
	< Back	Next>	Finish	Cancel		

- 2.7. Set the Family name: Select *Max7000S* from the drop-down menu in field (a).
- 2.8. Set the Speed grade: Select 8 from the drop-down menu in field (b).
- 2.9. Set the **Pin count**: Select **84** from the drop-down menu in field (c).
- 2.10. Select *EPM7128SLC84-7* from the available devices in field (d).

Note: These settings are only used when implementing the Altera Max chip on the UP2 Board. The Altera Flex on the UP2 and the Altera Cyclone on the UP3 Board have different settings.

- 2.11. Click *Next* at the bottom of page 3 of the New Project Wizard.
- 2.12.Click *Next* at the bottom of the **EDA Tool Settings** (page 4). *You will now be on Summary page as shown below.*

New Project Wizard: Summary	[page 5 of 5]			×
When you click Finish, the proje	ct will be created	with the following	g settings:	
Project directory:				
C:/rive5663/csc343/mux_q	uartus/			
Project name:	mux_2input			
Top-level design entity:	mux_2input			
Number of files added:	1			
Number of user libraries added:	0			
Device assignments:				
Family name:	MAX7000S			
Device:	EPM7128SLC8	34-7		
EDA tools:				
Desian entru/sunthesis:	<none></none>			
Simulation:	<none></none>			
Timing analysis:	<none></none>			
rinning analysis.	(Hono)			
	< Back	Next>	Finish	Cancel

- 2.13. Click *Finish* at the bottom of page 5 of the **New Project Wizard**.
- 3. Create a new block diagram file(.*bdf*).
 - 3.1. Click *File->New*.

A new window appears like the one below.

New	x
Device Design Files Software Files Other Files	
Block Diagram/Schematic File	
EDIFFile Verilog HDL File VHDL File	
OK Cancel	

3.2. Select the *Block Diagram/Schematic File* option and click *OK*. *A new window appears like the one below.*

🕞 🔡 ВІ	lock1.bdf
A	
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Symbol Tool	Block1.bdf
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<u>/</u>]	
4	
4	

3.3. Select the *Symbol Tool* from the toolbar on the left of the block diagram. *A new window appears like the one below.*



- 3.4. Click on *primitives -> logic -> and2* to get the and symbol and click *OK*. *The cursor now acts as a stamp in the block diagram window. It will stamp an and gate every time you click inside the window.*
- 3.5. Place two and gates inside the block diagram window referencing the Multiplexer schematic below.

3.6. Right-click inside the block diagram window or click on the *Selection and Smart Drawing Tool* at the top of the toolbar to finish using the *and* gate.

Note: You can delete mistakes by right-clicking on an object and selecting Delete.



3.7. Place one *or2* symbol and one *not* symbol in the block diagram window referencing the schematic above.

Note: These symbols can be found in the same place as and2..

3.8. Place three *input* pins and one *output* pin in the block diagram window according to the schematic above.

Note: These symbols can be found in *primitives -> pin* in the Symbol window.

3.9. Select the **Orthogonal Node Tool** from the toolbar on the left as shown below.



- 3.10. Connect each object as shown in the schematic above:
 - a) Click as close as possible to one object.
 - b) Drag the connection toward a second object until a small box appears.

Note: A unconnected wire shows an X along the wire when the wire is not highlighted.

- 3.11. Name each pin:
 - a) Double click on the upper left-most *input* pin.
 - b) Type *Sel* in the **Pin name(s)** field and click *OK*.
 - c) Name the second *input* pin *I0* and the third *input* pin *I1*.
 - d) Name the *output* pin *O*.
- 3.12. Save the file as *multiplexer.bdf*.

- 4. Create a symbol to represent the above file:
 - 4.1. Click inside the *multiplexer.bdf* to make sure this is the active window.
 - 4.2. Click *File -> Create/Update -> Create Symbol Files for Current File* as in the figure below.

Note: Make sure the *multiplexer.bdf* file is highlighted before creating the symbol.

	New Ctrl+N	💦 🕅 🕅 🕅 Mux_2input
	Open Ctrl+O Close Ctrl+F4	multiplexer.bdf
	New Project Wizard Open Project Ctrl+J Convert MAX+PLUS II Project Save Project Close Project Save Ctrl+5 Save As Save Current Report Section As	
	Eile Properties	
	Create / Update 🔹 🕨	Create HDL Design File for Current File
	Export ₂ Convert Progra <u>m</u> ming Files	Create Symbol Files for Current File Create AHDL Include Files for Current File
	Page Setyp Print Pre <u>v</u> iew	Create Design File from Selected Block Update Design File from Selected Block
4	Print Ctrl+P Recent Files	Create SignalTap II File from <u>D</u> esign Instance(s) Create SignalTap II List File
	Recent Projects	Create JAM, SVF, or ISC File Create/Update IPS File
	E <u>x</u> it Alt+F4	

5. Click on the *Files* tab in the **Project Navigator** window shown below.



- 6. Double-click on *DEC_7SEG.vhd* to open the file.
- 7. Create a symbol for this file as well using the process described above.
- 8. Create a new block diagram file:
 - 8.1. Repeat steps 5.1, 5.2, and 5.3. *A new* **Project** *folder will appear above the altera libraries folder as shown in the*



- 8.2. Click on the **Project** folder, select *dec_7seg* and click *OK*.
- 8.3. Place one *dec_7seg* symbol in the block diagram referencing the schematic below.



- 8.4. Place one *Multiplexer* symbol in the block diagram.
- 8.5. Place three *input* pins and seven *output* pins as shown in the schematic above.

- 8.6. Connect all objects as shown above using the Orthogonal Node Tool.
- 8.7. Name all pins in the following order from top to bottom, left to right: Input: S, I0, I1 Output: O, a, b, c, d, e, f, g
- 8.8. Save the file as mux 2input.bdf.
- 9. Compile your design:
 - 9.1. Click *Processing -> Start Compilation* as shown below. *Quartus will show the status of the compilation process in the* **Status** *window on the left side of the screen and will show a confirmation of completion.*



9.2. Click *OK* in the confirmation window and exit out of the Compilation Report window that is shown below.



- 10. Create a vector waveform file (**.vwf**):
 - 10.1. Click *File -> New*, and click on the **Other Files** tab as shown below.

lew	x
Device Design Files Software Files Other Files AHDL Include File Block Symbol File Chain Description File Hexadecimal (Intel-Format) File Memory Initialization File SignalT ap II File Tol Script File Text File Vector Waveform File	
OK Cancel	

10.2. Select Vector Waveform File.

A new window will appear as shown below.

Gaveform1.vwf			
Master Time Bar: 11.55 ns	Pointer: 300 ps	Interval: -11.25 ns Start:	End:
Name	0 ps	10.0 ns	20.0 ns
Name		11.55 ns 1	
Cut	⊂trl+X		
Сору	Ctrl+C		
Paste	Ctrl+V		
Paste Special			
Repeat Paste			
Delete	Del		
Insert Copied No	des		
Insert Node or	r Bus		
Zoom	•		

10.3. Right-click under the **Name** field in the left section of the waveform window and select **Insert Node or Bus**.

A new window will appear as shown below.

Insert Node o	or Bus	×
Name:		OK
Туре:	INPUT 💌	Cancel
Value type:	9-Level	Node Finder
Radix:	Binary 💌	
Bus width:	1	
Start index:	0	
🗖 Display gr	ay code count as binary count	

10.4. Select **Node Finder** on the right side of the window. *A new window will appear as shown below.*

Node Finder		×
Named: ×	Filter: Pins: all	List OK
Look in: mux_2input		🔽 🗹 Include subentities 🛛 Stop 🍼 Cancel
Nodes Found:		Selected Nodes:
Name	Assignments Type	Name Assignments T
💿 a	Unassigned Output	
🐵 Ь	Unassigned Output	
🗇 c	Unassigned Output	
d 💿 d	Unassigned Output	
💿 e	Unassigned Output	
🐵 f	Unassigned Output	
💿 g	Unassigned Output	
I0 I 0	Unassigned Input	
I1 II	Unassigned Input	>>>
IIII IIII IIII IIII IIII IIII IIII II	Unassigned Input	

- 10.5. Click on the **List** button the right side of the window. All input and output pins in the design will appear in the left window as show above.
- 10.6. Select S then click on the > button in the middle of the window.
- 10.7. Repeat step 12.6 for IO, I1, and O in that order.

10.8. Click *OK* to exit the **Node Finder** window and *OK* again to insert these items into the vector waveform as shown below.



- 10.9. Click on **I1** and select the **Forcing High** button from the toolbar on the left. *This sets I1 to always input 1 as seen above.*
- 10.10. Click and drag over the interval from 10.0ns to 20.0ns in the S signal and select the **Forcing High** button.

This produces a step in the signal shown below.

A	🔡 mux_2input.	bdf	mux_2input.vwf*			vf*
Æ€	Master Time Bar:	0 ps	• •	Pointer:	4.5 ns	Interval:
			0 ps	10.0 ns	20	.0 ns
# 1 3		Name				
<u>\</u> v 💥	S					L
압 ,			<u> </u>			
Z VE VE	rcing High (1)			*****	*******	*******

10.11. Save the file as *mux_2input.vwf*.

11. Simulate your design:

11.1. Click *Processing -> Start Simulation* as shown below.



11.2. Click *OK* once the confirmation window appears, but DO NOT exit out of the **Simulation Report** window.

Note: The Simulation Report window shows the output of your design.

- 11.3. Analyze the output in the **Simulation Report**. Notice that when **S** is 0, the output is whatever **I0** is, and when **S** is 1, the output is whatever **I1** is.
- 12. Download your design onto the chip:
 - 12.1. Click Assignments -> Import Assignments.



12.2. Click on the ... button in the Import Assignments window to browse for the mux_2input_pin_assignment file you copied at the beginning of the lab and click OK.

Import Assignments	×							
Specify the source and categories of assignments to import. Click LogicLock Impo to select LogicLock Import File(s).	rt File Assignments							
Assignment source	Ceterrories							
File name: /CSC 342 Fall 06/mux_2input_pin_assignment.csv	Categories							
O Use LogicLock Import File Assignments	Advanced							
LogicLock Import File Assignments								
Copy existing assignments into mux_2input.qsf.bak before importing								
ОК	Cancel							

12.3. Save your design and recompile to include the pin assignments. Click *Tools -> Programmer*.

A new window appears as show below.

Ardware Setup ByteBlasterII [LPT1]				Mode: JTAG			Progress	:	0%
🏓 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit
🖿 Stop	mux_2input.pof	EPM7128SL84	001D7D2A	0000FFFF	✓				
\mu Auto Detect									
🗙 Delete									
📛 Add File									
👺 Change File									
🔛 Save File									
🗳 Add Device									

12.4. Click Hardware Setup and make sure that the ByteBlaster(MV) hardware is listed.

If it is not listed,

- a) Click Add Hardware and select ByteBlaster(MV) for the Hardware Type
- b) Select Parallel Port LPT1 and click OK.

12.5. Click on the Program/Configure checkbox of your mux2_input.pof file in the

Programmer window and click **Start**.

If your file is not listed in the window, click Add File, select your file and click OK.

13. Compare your results on the board with that of the waveform. Try as many combinations as you can and see how many outputs you can get to display correctly.